What is claimed is:

1. A method of manufacturing a semiconductor integrated circuit device including a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix of a plurality of rows and columns, the method comprising the following steps (a) to (k):

(a) a step of forming an element isolation region on the surface of a semiconductor layer;

(b) a step of forming a first gate insulating layer and a laminate having a first conductive layer for a word gate disposed over the first gate insulating layer on the semiconductor layer, the laminate having a plurality of openings extending in a first direction;

(c) a step of forming second gate insulating layers on the semiconductor layer so as to be adjacent to both sides of the first gate insulating layer;

(d) a step of forming side insulating layers on both sides of the first conductive layer for the word gate;

(e) a step of forming a second conductive layer over the entire surface of a structure formed by the steps (a) to (d) so as to cover the structure;

(f) a step of forming a first mask layer on the second conductive layer at least in a region in which a common contact section is formed;

(g) a step of forming a control gate and a common contact section which comprises:

anisotropically etching the entire surface of the second conductive layer to form first and second control gates in the shape of sidewalls continuous in the first direction on either side of the side insulating layers, and to form a contact conductive layer at least in a region in which the common contact section is formed; and

forming the contact conductive layer continuously with a pair of the first and second control gates adjacent in a second direction which intersects the first direction;

(h) a step of doping the semiconductor layer located between the first and second control gates with impurities, and forming an impurity diffusion layer which forms a source region or a drain region;

(i) a step of forming an insulating layer which covers the first and second control gates;

(j) a step of forming a second mask layer in a region in which the common contact section is formed; and

(k) a step of patterning the first conductive layer for the word gate.

2. The method of manufacturing a semiconductor integrated circuit device according to claim 1,

wherein the second conductive layer for the control gate is formed of a doped polysilicon layer.

3. The method of manufacturing a semiconductor integrated circuit device according to claim 1,

wherein the second gate insulating layer is formed by depositing a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer one after another.

4. The method of manufacturing a semiconductor integrated circuit device according to claim 3,

wherein the side insulating layers is formed in the same step as a step of forming the first silicon oxide layer, the silicon nitride layer, and the second silicon oxide layer.

5. The method of manufacturing a semiconductor integrated circuit device according to claim 3,

wherein the common contact section comprises an insulating layer formed on the semiconductor layer, and the insulating layer is formed in the same step as a step of forming the first silicon oxide layer, the silicon nitride layer, and the second silicon oxide layer.

6. The method of manufacturing a semiconductor integrated circuit device according to claims 1,

wherein the step (b) comprises a step of forming a stopper layer for chemical mechanical polishing on the first conductive layer for the word gate, and

wherein in the step (i), the insulating layer which covers the first and second control gates is provided by forming an insulating layer on the entire surface of the structure formed by the steps (a) to (h) and then removing the insulating layer

by chemical mechanical polishing until the stopper layer is exposed.

7. The method of manufacturing a semiconductor integrated circuit device according to claim 6,

wherein the stopper layer is formed so that an upper surface thereof is located at a position higher than an upper end of the control gate.

8. The method of manufacturing a semiconductor integrated circuit device according to claim 7,

wherein the side insulating layers is formed so that an upper end thereof is located at the same level as an upper surface of the stopper layer.

9. The method of manufacturing a semiconductor integrated circuit device according to claims 1,

wherein the common contact section is provided adjacent to an end of the impurity diffusion layer.

10. The method of manufacturing a semiconductor integrated circuit device according to claim 1,

wherein the common contact sections are staggered relative to each other.

11. The method of manufacturing a semiconductor integrated circuit device according to claims 1,

wherein the memory cell array is divided into a plurality of blocks.

12. The method of manufacturing a semiconductor integrated circuit device according to claim 11,

wherein contact impurity diffusion layer is formed in the semiconductor layer after the step (a), and the impurity diffusion layer in one of the blocks is connected to the impurity diffusion layer in another one of the blocks adjacent to the one block through the contact impurity diffusion layer.

13. The method of manufacturing a semiconductor integrated circuit device according to claims 1,

wherein the first mask layer is formed corresponding to a region in which the common contact section is formed in the step (f).

14. The method of manufacturing a semiconductor integrated circuit device according to claims 1,

wherein in the step (f), the first mask layer is formed continuously so as to cover regions in which a plurality of the common contact sections arranged in the second direction are formed.

15. The method of manufacturing a semiconductor integrated circuit device according to claim 14,

wherein in the step (g), a conductive layer is continuously

formed so as to include regions in which the common contact sections are formed, by the first mask layer, and

wherein in the step (k), the contact conductive layer is formed together with the word gate by patterning the conductive layer together with the first conductive layer.